Atty. Docket No. PIA31223/DBE/US
Serial No: 10/751,212

Remarks

Applicant and his representatives wish to thank Examiner Ha for the thorough examination of the present application, and the detailed explanations in the Office Action dated June 16, 2005. Applicant has carefully reviewed the Examiner's Office Action.

The present invention relates to a method for packaging a semiconductor device, including the steps of (a) forming an Au bump on a bond pad of a wafer, (b) dicing the wafer into a chip, and (c) attaching the Au bump of the chip to a substrate to form a flip-chip bond by using a thermo-pressure process. Therefore, the typical flip-chip attachment process of attaching solder balls to the substrate is not required, which eliminates subsequent flux printing and deflux processes. The present invention thereby enables miniaturization of the semiconductor device, simplification of the packaging process, and reduced costs.

The references cited by the Examiner (Farnworth [US 2004/0104473] and Matsushima [US 6,232,652]) neither disclose nor suggest attaching an Au bump on the bond pad of a wafer to a substrate using a thermo-pressure process.

The Rejection of Claims 1 and 2 under 35 U.S.C. § 103(a)

The rejection of Claims 1 and 2 under 35 U.S.C. § 103(a) as being unpatentable over Farnworth in view of Matsushima is respectfully traversed.

Farnworth relates to a method of forming bond pads (e.g. contact pad 34) that are encapsulated (e.g. encapsulating layer 40) in a semiconductor chip die (e.g. chip die 10). Farnworth further discloses a method for attaching the bond pads of the chip die to a substrate using a wire-bonding process (e.g. FIGS. 3A and 3B, and page 4, paragraph 55). Farnworth also suggests that the disclosed bond pads may alternatively be used in a flip chip bonding process, but does not disclose details of such a process. (See, e.g. Farnworth, page 4, paragraph 58.) A typical flip chip bonding process does not include the steps of forming an Au bump on a bond pad and attaching the Au bump of the chip to a substrate using a thermo-pressure process. A typical flip chip bonding process includes the steps of forming solder balls (e.g. using high lead

solder, especially 95 Pb:5 Sn) on the bond pads, flipping the chip over to place the solder balls in contact with the substrate, and applying a reflow process to attach the solder balls to the substrate. (See, e.g., S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Volume 1 – Process Technology (2nd ed. 2000), pp. 857-858.) (More recently, the industry has begun to move away from Pb to Pb-free solder balls. See Electronic News, IPC Determines Replacement for Lead Solder, July 4, 2005, attached hereto.) Therefore Farnworth does not disclose or suggest forming an Au bump on a bond pad and attaching the Au bump of the chip to a substrate using a thermo-pressure process.

Matsushima relates to a semiconductor device including a substrate, a semiconductor chip mounted approximately in the center of the semiconductor device, and annular rings and a heat spreader that may be attached to the substrate around the chip using a thermal pressure bonding process. Matsushima discloses that the chip may be flip-chip-bonded to the substrate *via solder bumps*. (See, e.g., Matsushima Col. 3, lies 20-22.) Matsushima, therefore, does not disclose or suggest the use of a thermo-pressure process to attach a chip with Au bumps to a substrate. By using a typical solder reflow process to attach the chip to the substrate, while using the thermal pressure bonding process to attach the rings and the heat spreader, Matsushima appears to teach or lead one away from attaching a chip to a substrate using a thermo-pressure process.

Neither Farnworth nor Matsushima discloses forming an Au bump on a bond pad and attaching the Au bump of the chip to a substrate using a thermo-pressure process. Therefore a combination of the two references cannot disclose or suggest all of the limitations of Claim 1, and the rejection under 35 U.S.C. § 103(a) of Claims 1 and 2 as being unpatentable over Farnworth in view of Matsushima should be withdrawn.

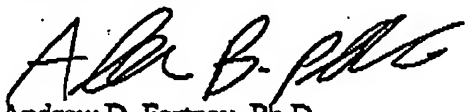
Atty. Docket No. PIA31223/DBE/US
Serial No: 10/751,212

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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